REMARKS

This Amendment is responsive to the Office Action of September, 2004. Claim 35 has been amended. Claims 1 – 39 remain pending in this application. Reexamination and reconsideration are respectfully requested.

The Examiner rejected Claims 1, 6 – 9, 30 and 35 under 35 USC 102(b) as being anticipated by Pan (6,259,139). This rejection is respectfully traversed.

The present invention is directed to an integrated circuit incorporating an ESD protection circuit which addresses the problem of thermo-mechanical damage which is introduced into an ESD circuit during ESD events. This is in contrast to prior art approaches which focus on electrical breakdown characteristics of ESD circuit structures and completely ignore the thermo-mechanical damage which can result due to heating which occurs during the ESD events. For example such thermo-mechanical damage can include cracking due to the thermal expansion characteristics of semiconductor materials employed in such circuits, and in particular silicon, which introduce thermally-induced mechanical stress into the crystal silicon structure used for the substrate and active devices forming the ESD circuit. Although purely thermal ESD effects (device failure or melting due to excessive heating) have been considered in the art and addressed, e.g. through heat sinks or heat reservoir structures, the thermo-mechanical problems have remained completely unrecognized and no ESD circuits or structures specially adapted for their thermo-mechanical properties have been incorporated in ESD circuits. The present invention addresses this heretofore unrecognized problem by incorporating materials with thermo-mechanical properties specially adapted to resist thermo-mechanical damage into the ESD circuit. Such never

previously recognized properties include, for example, thermal expansion coefficient, mechanical strength and fracture toughness (resistance to cracking).

The Pan reference is directed to a MOS ESD protection circuit which is completely consistent with conventional prior art approaches in that it focuses on electrical characteristics of the ESD circuit active device regions and surrounding substrate regions not the thermo-mechanical properties of the structures. At numerous locations the Pan reference emphasizes the "electricity" characteristics of the various regions (for example, Abstract, last two sentences, col. 3, lines 40-44, etc.). There is nothing whatsoever in the Pan reference to suggest that any of the separate regions which are identified as part of the ESD overall device structure, including the substrate 30, would be selected from a material chosen for its thermo-mechanical properties. The Examiner cited col. 4, l. 38-40 of the Pan reference for his assertion that the substrate 30 is a thermal energy absorbing region made from a material substantially more resistant to thermo-mechanical expansion than the active device region. However, this portion of the Pan reference is actually describing the electrical characteristics of the substrate and since it comprises a large volume it can act as a heat reservoir. Nothing in this discussion states or even suggests that the substrate has different thermal-mechanical properties than the active device region. To the contrary, it seems clear from the reference as a whole that the various regions comprising the ESD circuit identified in figures 3A and 3B of the Pan reference are simply different doping regions of a semiconductor substrate (likely silicon) as in conventional MOS ESD protection circuits (see, e.g. Abstract last two sentences). Accordingly, it is respectfully submitted that the Pan reference fails to disclose the invention as claimed and the rejection is fully traversed.

The Examiner rejected Claims 2 – 5, 10, and 32 – 34 under 35 USC 103(a) as being unpatentable over Pan (6,259,139) as applied to Claim 1, and further in view of Yatsuo et al. (6,353,236). This rejection is respectfully traversed.

The Examiner cited the Yatsuo et al. reference as teaching a SiC material stating it would be obvious to combine the Yatsuo et al. reference with Pan as an obvious substitution for Pan's "thermal energy absorbing layer". However, this rejection is premised on the incorrect interpretation of Pan as teaching a "thermal energy absorbing layer" having different thermo-mechanical properties than the active region (and in particular different thermal expansion properties as set out in claim 1) and that it would be obvious to optimize these properties. But, as noted above the thermo-mechanical properties of the "thermal energy absorbing layer" of Pan are not different than his active regions, simply the electrical properties are different. Therefore, there is nothing to suggest optimizing the thermo-mechanical properties of the "thermal energy absorbing layer" of Pan using the Yatsuo et al. reference, or any other reference, as proposed by the Examiner. Accordingly, there is nothing but hindsight and the teachings of the present invention to motivate the combination. Since these motivations are insufficient to support a prima facie 103 rejection it is respectfully submitted this rejection is also fully traversed.

The Examiner rejected Claims 11 and 31 under 35 USC 103(a) as being unpatentable over Pan (6,259,139) as applied to Claim 1, and further in view of Uenishi (2002/0070424). This rejection is respectfully traversed. The Examiner cited the Uenishi reference as disclosing a resistor in an ESD circuit which he stated could be combined with the ESD circuit of Pan. Even if true, however, due to the deficiencies of Pan discussed above the present invention as claimed would not be the result. Accordingly,

it is respectfully submitted this rejection is fully traversed for the reasons discussed above.

The Examiner rejected Claims 22 – 29 and 36 – 39 under 35 USC 103(a) as being unpatentable over Pan (6,259,139) in view of Yatsuo et al. (6,353,236). This rejection is respectfully traversed.

This rejection is premised on the same interpretation of the Pan and Yatsuo et al. references relied on by the Examiner in relation to the rejection of Claims 2 – 5, 10, and 32 – 34. As discussed above the Examiner's reasons for concluding that there is a suggestion for their combination in the references themselves is based on a misinterpretation of Pan. Therefore, the proposed combination equally fails for the 103 rejection of Claims 22 – 29 and 36 – 39 and it is respectfully submitted this rejection is also fully traversed.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully requested. It is requested that the Examiner telephone the undersigned attorney if it appears that any impediment remains to allowance of the application.

Respectfully submitted,

Date: 12/20/04

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